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Atty. Docket No. **970813**
Date August 29, 1997

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

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Transmitted herewith for filing is the patent application of

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For: **FABRICATION METHOD OF SEMICONDUCTOR DEVICE AND ABRASIVE LIQUID USED THEREIN**

XX Specification - 33 pages, Claims - 7 pages, Abstract - 1 page.

XX Drawings - 14 sheets of drawings.

XX Declaration and Power of Attorney.

XX An assignment of the invention to SANYO ELECTRIC CO. LTD.

XX Priority of Japanese Applns. Nos. 8-230826 and 9-010426 respectively filed on August 30, 1996 and January 23, 1997 are claimed under 35 USC 119, 2 certified copies of which are attached hereto.

XX Information Disclosure Statement with attached Form PTO-1449 (2 references).

XX A filing fee, calculated as shown below:

	Number Filed	Number Extra	Rate	Basic Fee $770.00
Total Claims	30 - 20	10	x 22.00	220.00
Independent Claims	5 - 3	2	x 80.00	160.00
Multiple Dependent Claims			260.00	
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment				40.00
TOTAL				$1190.00

XX Our check in the amount of **$1,190.00** for patent application processing fees under 37 CFR 1.16 is enclosed. ($1,150.00 for filing fee and $40.00 for Assignment Recordation fee).

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Enclosures: Spec.; Clms.; Abstr.; Decl.; Assign.; Draws. (14 sheets); Claim for Priority (2 cert. copies); IDS w/PTO-1449 (2 refs).

TITLE OF THE INVENTION

Fabrication Method of Semiconductor Device and Abrasive Liquid Used Therein

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of fabricating a semiconductor device, and abrasive liquid used therein. More particularly, the present invention relates to a fabrication method of a semiconductor device including the step of planarizing an insulation film, and abrasive liquid used therein.

Description of the Background Art

Reducing the size of interconnections and providing multilayers are now required to further increase the integration density of semiconductor integrated circuit devices. An interlayer insulation film is provided between each interconnection to obtain a multilayer structure of the interconnection. If the surface of this interlayer insulation film is not planar, a step-graded portion will be generated at the interconnection formed above the interlayer insulation film. This will cause defects such as disconnection.

Therefore, the surface of the interlayer insulation film (the surface of the device) must be made as flat as possible. The technique to planarize the surface of the

device is called planarization. This planarization technique has become important in reducing the size and providing multilayers of the interconnection.

The following two methods are known as conventional planarization techniques. As the first method, planarization using an SOG (Spin On Glass) film is known. The technique of planarization using an SOG film will be described hereinafter.

An SOG film is known as the most commonly used interlayer insulation film in the planarization art. In recent years, development in the planarization technique taking advantage of fluidity of a material of the interlayer insulation film is particularly noticeable.

An "SOG film" is a generic term of a film mainly composed of a solution in which a silicon compound is dissolved in an organic solvent, and silicon dioxide formed from that solution. In forming an SOG film, first a solution having a silicon compound dissolved in an organic solvent is applied in droplets while the substrate is rotated. By this rotation, the solution coating is provided so as to alleviate the step-graded portion on the substrate corresponding to the interconnection. More specifically, the coating is formed thick at the concave portion and thin at the convex portion on the substrate. Thus, the solution coating results in a planarized surface.

Heat treatment is then applied to vaporize the organic solvent. Also, polymerization proceeds to result in a planarized SOG film at the surface.

An SOG film is typically classified into an inorganic SOG film that does not include any organic component in the silicon compound, as represented by the following general formula (1), and an organic SOG film including an organic component in a silicon compound, as represented by the following general formula (2).

$$[SiO_2]_n \quad \ldots(1)$$

$$[R_x\ SiO_Y]_n \quad \ldots(2)$$

(n, X, Y: integer; R: alkyl group or aryl group

An inorganic SOG film has a disadvantage that it is more brittle than a silicon oxide film formed by CVD (Chemical Vapor Deposition) in addition to high hygroscopic. For example, a crack is easily generated during the heat treatment in an inorganic SOG film when thicker than 0.5μm.

In contrast, although an organic SOG film is highly hygroscopic, the organic SOG film is suppressed in generation of a crack during heat treatment. Therefore, the organic SOG film can be formed to a thickness to approximately 0.5-1.0μm. That is, The usage of an organic SOG film allows the formation of a thicker interlayer insulation film. Therefore, sufficient planarization can

be achieved even for a great step-graded portion on a substrate.

The second method of planarization employs chemical mechanical polishing (referred to as CMP hereinafter).

The CMP method is a process including chemical action in addition to mechanical polishing. For example, after a thick insulation film such as of silicon oxide is formed on a substrate by plasma CVD and the like, the insulation film is polished down to a predetermined film thickness by CMP. In this CMP method, polishing is carried out while applying an abrasive with colloidal silica as the main component.

Planarization using an SOG film is advantageous over one using an insulation film deposited only by CVD in that favorable planarization is achieved. However, this planarization of the current level in which complete planarization cannot be achieved is not sufficient to meet the potential high standard for an interlayer insulation film as microfabrication proceeds and the scale of integration increases since an SOG film is formed from liquid. It is therefore difficult to completely correspond to the microfabrication and high integration of the devices.

Planarization according to CMP is advantageous over planarization using SOG film in that planarization of a

higher level can be achieved. However, when only an insulation film (for example, a silicon oxide film) formed by CVD is used as an interlayer insulation film as in the conventional case, it is difficult to embed an insulation film in microminiaturized interconnection without any gap. A void may be generated. Even if the interconnections are filled with an insulation film without any gap, the capacitance between the interconnections will become greater since the insulation film formed by CVD has a high relative dielectric constant. This causes the problem that the operating speed of the LSI will be degraded due to RC delay.

An approach of achieving a favorable planarized surface of an appropriate level by planarization using an SOG film, and then polishing the planarized surface by CMP for further planarization is conventionally known.

However, this process of polishing an SOG film by CMP induces problems set forth in the following. The polishing rate of an SOG film by CMP is lower than that of the case where an insulation film formed by CVD is polished by CMP. Therefore, the throughput is reduced to increase the cost for fabrication. There is also a problem that a defect such as a scratch (generated during polishing) is easily generated at the surface of the SOG film.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a fabrication method of a semiconductor device that allows improvement in planarization and polishing rate of an insulation film.

Another object of the present invention is to provide a fabrication method of a semiconductor device that can effectively prevent a defect from being generated in an insulation film during polishing working thereof.

According to an aspect of the invention, a fabrication method of a semiconductor device includes the following steps. First, impurities are introduced into a first insulation film. Then, planarization is carried out by polishing the surface of the first insulation film in which impurities are introduced. By carried out polishing after impurities are introduced into the first insulation film, the polishing rate of the first insulation film by CMP is improved substantially to a level equal to the polishing rate of a silicon oxide film formed by CVD. Accordingly, the polish workability can be improved. Since polishing of the first insulation film is promoted by introduction of impurities thereto, the problem of generation of a defect such as a scratch during polishing of the first insulation film can be prevented effectively.

According to another aspect of the present invention, a method of fabricating a semiconductor device includes

the following steps. A first insulation film is formed on a substrate. Then, a second insulation film is formed on the first insulation film. Impurities are introduced to at least the surface of the first insulation film before or after formation of the second insulation film. Planarization is achieved by polishing at least the second insulation film. By introducing impurities to at least the surface of the first insulation film, the portion where impurities are introduced has a polishing rate by CMP as high as that of a silicon oxide film formed by CVD. As a result, the polish workability of the first insulation film is improved. Also, a defect such as a scratch is not easily generated. In the fabrication method of the present aspect, the step of planarization can be carried out by polishing the first and second insulation films. The second insulation film can include a silicon oxide film formed by plasma CVD. Also, a photoresist film can be formed on the surface of a device before introducing impurities to the first insulation film, and introduce impurities to the first insulation film via the photoresist film. As a result, the depth of the introduced impurity is substantially set uniform since impurities are introduced via a photoresist that has an extremely flat surface. This provides the advantage that the boundary depth between the portion of the first insulation film

where impurities are introduced and the portion where impurities are not introduced became uniform so that the end point for polishing can easily be detected by virtue of the portion without impurity introduced serving as a stopper with respect to polishing. In the fabrication method of the present aspect, a third insulation film can be formed on the surface of the device after polishing, and a fourth insulation film can be formed on the surface of the device prior to formation of the first insulation film. The formation of the third and fourth insulation films provides the advantage of increasing the mechanical strength of the insulation film. Also, the first insulation film can include a silicon oxide film material consisting of at least 1% of carbon in the fabrication method of the present aspect. Furthermore, the first insulation film can include a material having a contact angle of 30°C and below of purified water with respect to the first insulation film. The first insulation film can also include an inorganic SOG film. The above-described polishing can be carried out according to chemical mechanical polishing. In this case, a surfactant is preferably used in the polishing step. It is also preferable to introduce impurities to the first insulation film by implantation. In this case, the impurities preferably include at least one element selected from the

group consisting of argon, boron, nitrogen and phosphorus.

A method of fabricating a semiconductor device according to another aspect of the invention includes the following steps. First, a first insulation film is formed on an substrate. Impurities are introduced into at least a surface of the first insulation film. Planarization is effected by polishing the first insulation film. The introduction of impurities to at least the surface of the first insulation film provides the advantage that the portion of the first insulation film in which impurities are introduced is improved in the polishing rate. Also, generation of a defect such as a scratch during polishing can be prevented effectively. According to the fabrication method of the present aspect, impurities can be introduced only to the surface of the first insulation film. Also, a third insulation film can be formed on the surface of the device after polishing, or a fourth insulation film can be formed on the surface of the device before the first insulation film is formed. Formation of the third and fourth insulation films provides the advantage that the mechanical strength of the entire insulation film is improved. The first insulation film can include a silicon oxide material containing at least 1% of carbon. The first insulation film can include a material having a contact angle of not more than 30°C of purified water with respect

to the film. The first insulation film can include an inorganic SOG film. Also, the above polishing step can be carried out by chemical mechanical polishing. In this case, an abrasive liquid including a surfactant is preferably used. Impurities can be introduced into the first insulation film by implantation. In this case, the impurities preferably include at least one element selected from the group consisting of argon, boron, nitrogen and phosphorus.

A fabrication method of a semiconductor device according to still another aspect of the present invention includes the following steps. First, a first insulation film is formed on a substrate. A second insulation film is formed on the first insulation film. Planarization is effected by polishing at least the second insulation film using abrasive liquid including a surfactant according to chemical mechanical polishing. By using abrasive liquid including a surfactant in chemical mechanical polishing, abrasive liquid of favorable wettability can be obtained to carry out the polishing work more favorably. In this case, the surfactant is preferably a fatty acid compound. Impurities can be introduced to the first insulation film after this polishing step.

The abrasive liquid according to still another aspect of the present invention includes at least a surfactant

used in a chemical mechanical polishing process. In this case, the surfactant preferably includes a fatty acid compound.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-7 are sectional views of a semiconductor device for describing a fabrication method thereof according to a first embodiment of the present invention.

Fig. 8 is sectional view of a semiconductor device for describing a fabrication method thereof according to a second embodiment of the present invention.

Figs. 9-14 are sectional views of a semiconductor device for describing a fabrication method thereof according to a third embodiment of the present invention.

Figs. 15-19 are sectional views of a semiconductor device for describing a fabrication method according to a fourth embodiment of the present invention.

Figs. 20-23 are diagrams for describing the characteristics of an embodiment of the present invention.

Fig. 24 is a schematic diagram for describing an embodiment of the present invention.

Fig. 25 is a diagram for describing the characteristics of an embodiment of the present invention.

Figs. 26-32 are sectional views of a semiconductor device for describing a fabrication method thereof according to a sixth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described hereinafter with reference to the drawings.

First Embodiment

A fabrication process of a semiconductor according to a first embodiment of the present invention (first to seventh steps) will be described with reference to Figs. 1-7.

In the first step of Fig. 1, a silicon oxide film 2 is formed to a thickness of approximately 300-800nm at the surface of a silicon substrate 1. Silicon oxide film 2 is formed so as to cover a gate electrode (not shown) and the like on silicon substrate 1. Silicon oxide film 2 can be formed according to an arbitrary method such as oxidation, CVD, and PVD.

A metal film (not shown) is formed by magnetron sputtering on silicon oxide film 2. This metal film is patterned to form a metal interconnection 3. Metal interconnection 3 has a layered structure of TiN (film thickness 20nm)/Ti (film thickness 30nm)/AℓSiCu alloy

(film thickness 550nm)/TiN (film thickness 100nm)/Ti (film thickness 50nm) from the upper layer to the lower layer.

In the second step shown in Fig. 2, plasma CVD is carried out using TEOS (Tetra-ethoxy Silane:$Si(OC_2H_5)_4$) and oxygen to form a plasma TEOS oxide film 4 to a thickness of approximately 200nm on metal interconnection 3. The film thickness of plasma TEOS oxide film 4 is adjusted according to the underlying step-graded portion. Plasma TEOS oxide film 4 is formed thick at a great underlying step-graded portion and thin at a small underlying step-graded portion.

In the third step shown in Fig. 3, an organic SOG film 5 is formed on plasma TEOS oxide film 4. Organic SOG film 5 has a composition of $[CH_3Si(OH)_3]$. The total film thickness of organic SOG film 5 without the presence of a pattern is approximately 400nm.

Organic SOG film 5 is formed as set forth in the following. First, an alcohol based solution of a silicon compound of the above composition (for example, IPA+acetone) is applied on substrate 1 in droplets while the substrate is rotated for 20 seconds at the rotational speed of 2300 rpm. As a result, a coating of this solution is formed on substrate 1. This alcohol based solution coating is formed so as to alleviate the step-graded portion on substrate 1 by being formed thick at the

concave portion and thin at the convex portion. As a result, the surface of the alcohol based solution coating is planarized.

Then, in an atmosphere of nitrogen, a heat treatment is sequentially carried out for 1 minute at 100°C, 1 minute at 200°C, 1 minute at 300°C, 1 minute at 22°C, and 30 minutes at 300°C. By this sequential heat treatment, the alcohol system is vaporized and polymerization proceeds to form an organic SOG film of approximately 200nm in thickness with a planarized surface. By repeating the process starting from the coating step to the heat treatment step once more, an organic SOG film 5 having a thickness of approximately 400nm is obtained. This organic SOG film 5 is a silicon oxide containing at least 1% of carbon.

In the fourth step of Fig. 4, argon ions (Ar^+)6 are doped into organic SOG film 5 by ion implantation. This ion implantation is carried out under the conditions of a dosage of 1×10^{15}atms/cm^2 at the acceleration energy of 140Kev. As a result, ions are introduced to a depth of approximately 300nm from the surface layer of organic SOG film 5.

By implanting ions into organic SOG film 5, the organic component in the layer of organic SOG film 5 is decomposed, and the moisture and hydroxyl group included

in the film are reduced. As a result, the portion of organic SOG film 5 in which ions are implanted is modified into an SOG film 7 (referred to as a modified SOG film hereinafter) that does not include any organic component and that includes only a slight amount of moisture and hydroxyl group.

Fig. 20 shows results evaluated by subjecting organic SOG film 5 (untreated: unimplanted) and modified SOG film 7(ion implantation processed: Ar^+ - implanted) respectively to heat treatment for 30 minutes in an atmosphere of nitrogen according to TDS (Thermal Desorption Spectroscopy). In this case, ion implantation is carried out under the conditions of a dosage of 1×10^{15}atms/cm^2 and an acceleration energy of 140keV. Fig. 20 shows the amount of desorption for H_2O (m/e=18). It is appreciated from Fig. 20 that desorption of H_2O (m/e=18) is small for modified SOG film 7. This means that the moisture and the hydroxyl group included in organic SOG film 5 are reduced by the conversion of organic SOG film 5 into modified SOG film 7 by ion implantation.

Fig. 21 shows results of the evaluation of moisture in the film carried out for the purpose of detecting the hygroscopic property of organic SOG film 5 and modified SOG film 7. Organic SOG film 5 (untreated), organic SOG film 5 exposed to oxygen plasma (O_2 plasma), and modified

SOG film 7 (Ar^+) left in the atmosphere of a clean room were taken as the object. The amount of moisture in each film was indicated by the integrated density of the absorption (in the vicinity of $3500cm^{-1}$) of the O-H group in the infrared absorption spectrum using the FT-IR method (Fourier Transform Infrared Spectroscopy). The ion implantation was carried out under the conditions of a dosage of $1 \times 10^{15}atms/cm^2$ and an acceleration energy of 140keV.

It is appreciated from Fig. 21 that the moisture increases not only before and after the treatment, but even after 1 day when exposed to oxygen plasma. In contrast, modified SOG film 7 shows no increase in moisture after ion implantation. The increase in moisture is smaller than that of organic SOG film 5 even when left in the atmosphere of a clean room. In other words, modified SOG film 7 is less hydroscopic than organic SOG film 5.

Fig. 22 shows the result of a pressure cooker test (PCT) carried out for the purpose of detecting the moisture permeability of modified SO film 7 and organic SOG film 5. This pressure cooker test is a humidification test carried out in a saturated moisture ambient at 2 atmospheric pressure and 120°C in the present embodiment. The integrated intensity of the absorption peak (in the

vicinity of 3500cm^{-1}) of the O-H in organic SOG film 5 was obtained and plotted over the PCT time using the FT-IR method.

A specimen (AR^+ 20 keV) having only the surface modified by ion implantation was prepared and compared with a specimen having the film entirely modified (Ar^+ 140KeV) and with a specimen that was not modified (organic SOG film 5:untreated). When organic SOG film 5 not modified is subjected to the pressure cooker test, the absorption intensity in the vicinity of 35000cm^{-1} (of the O-H group) shows a significant increase. In modified SOG film 7, increase of the absorption intensity in the vicinity of 3500cm^{-1} (of the O-H group) is small. The increase in the specimen in which only the surface is modified is substantially equal to that of the film that is completely modified.

It is understood from the above results that a layer that has moisture permeability suppressed can be formed by implanting ions.

In the fifth step shown in Fig. 5, a plasma TEOS oxide film 8 is formed to a thickness of approximately 1-2μm on modified SOG film 7 according to a procedure similar to that of plasma TEOS oxide film 4.

In the sixth step shown in Fig. 6, the surface of the device formed according to the first to fifth steps is

polished by CMP. Here, an abrasive such as silica suspended into a potassium hydroxide aqueous solution or ammonia aqueous solution is used as the abrasive liquid.

Fig. 23 shows the polishing rate (the polish speed) when modified SOG film 7, organic SOG film 5, and plasma TEOS oxide film 8 (P-TEOS) are respectively polished by CMP. It is appreciated from Fig. 23 that modified SOG film 7 and plasma TEOS oxide film 8 have substantially an equal level of polishing rate, and that organic SOG film 5 has a polishing rate that is several times smaller than the polishing rate of modified SOG film 7 and plasma TEOS oxide film 8. Therefore, when plasma TEOS oxide film 8 is polished so as to expose modified SOG film 7 by CMP, plasma TEOS oxide film 8 and modified SOG film 7 are both modified uniformly since the polishing rate is substantially equal. Accordingly, the polished surface is rendered extremely planarized. Furthermore, a defect such as a scratch caused in polishing an SOG film that does not have ions introduced is not easily generated in polishing modified SOG film 7.

The polishing operation by CMP can be carried out until plasma TEOS oxide film 4 is exposed as shown in Fig. 6, or terminated before exposure (not shown).

The seventh step will be described with reference to Fig. 7. It may be thought that modified SOG film 7 left

after the sixth step of Fig. 6 does not have to have an insulation film further formed thereon since the water containing property and hygroscopic property are both extremely low. However, for the purpose of preventing any adverse effect from moisture included in the atmosphere and increasing the mechanical strength of the interlayer insulation film, a plasma TEOS oxide film 9 is formed to a thickness of approximately 200nm on the film planarized by CMP according to a procedure similar to that of plasma TEOS oxide film 4. Plasma TEOS oxide film 9 exhibits favorable planarization since the underlying plane is flat.

An upper interconnection not shown connected to metal interconnection 3 via a contact hole (via hole) is formed on plasma TEOS oxide film 9. Since the planarization of interlayer insulation film 10 formed of plasma TEOS oxide film 4, organic SOG film 5, modified SOG film 7, plasma TEOS oxide film 8 and plasma TEOS oxide film 9 is extremely favorable, the process for forming the upper interconnection can be carried out more easily. Also, the probability of disconnection in the upper interconnection is reduced significantly.

Second Embodiment

The fabrication method of a semiconductor device according to a second embodiment of the present invention differs from the fabrication method of a semiconductor

device of the first embodiment only in the step corresponding to the sixth step of the first embodiment shown in Fig. 6. The steps of the second embodiment corresponding to the first to fifth steps and the seventh step of the first embodiment are identical. Therefore, only the different step will be described for the second embodiment. The description of the remaining identical steps will not be repeated.

According to the second embodiment of the present invention, the surface of a device formed according to steps similar to those of the first to fifth steps of the first embodiment is polished by CMP as shown in Fig. 8. The polishing operation is terminated before modified SOG film 7 is exposed so that plasma TEOS oxide film 8 remains all over the device. As a result, the step corresponding to the seventh step of the first embodiment shown in Fig. 7 (the step of depositing plasma TEOS oxide film 9) can be omitted.

Since modified SOG film 7 will not be exposed in the polishing operation of the surface of the device by CMP in the second embodiment, the advantage of the high polishing rate of modified SOG film 7 cannot be utilized. However, organic SOG film 8 must be changed into modified SOG film 7 taking into account the probability of exposure of the SOG film due to polishing error. There is also a

possibility of contact failure in forming an electrode within a via hole if there is gas in the via hole from the SOG film, if exposed, at the side face of the via hole formed at a subsequent step. Organic SOG film 5 must be modified into SOG film 7 to prevent such disadvantages.

Third Embodiment

A fabrication method of a semiconductor device according to a third embodiment of the present invention will be described hereinafter with reference to Figs. 9-14. Components corresponding to those of the first embodiment have the same reference characters allotted, and detailed description thereof will not be repeated.

At the first step shown in Fig. 9, a silicon oxide film 2 is formed on the surface of a silicon substrate 1. A metal interconnection 3 is formed on silicon oxide film 2.

In the second step of Fig. 10, a plasma TEOS oxide film 4 is formed on metal interconnection 3.

At the third step of Fig. 11, an organic SOG film 5 is formed on plasma TEOS oxide film 4. Here, organic SOG film 5 is formed thicker than in the fabrication method of the first embodiment shown in Fig. 3. More specifically, following application of an organic SOG film to a thickness of 300nm, a heat treatment similar to that of the third step shown in Fig. 3 is carried out. By

repeating this process 4 to 5 times, an organic SOG film 5 is formed to have a total film thickness of approximately 1.2μm when there is no pattern.

At the fourth step shown in Fig. 12, argon ions (Ar^+) 6 are introduced by ion implantation into organic SOG film 5. The nature of the film is modified to result in a modified SOG film 7.

In the fifth step shown in Fig. 13, the surface of modified SOG film 7 is polished by CMP. This polish operation of modified SOG film 7 by CMP is carried out by a polishing rate substantially equal to that of a plasma TEOS oxide film. Since modified SOG film 7 is extremely low in hygroscopity, there is no adverse effect even when a great amount of abrasive liquid is used in the polish operation by CMP.

The sixth step will be described with reference to Fig. 14. It may be thought that an insulation film does not have to be formed on modified SOG film 7 since modified SOG film 7 left after the fifth step shown in Fig. 13 is extremely low in water containing property and hygroscopic property. However, for the purpose of preventing any adverse effect from moisture included in the atmosphere and to increase the mechanical strength as an interlayer insulation film, a plasma TEOS oxide film 9 is formed on modified SOG film 7 planarized by CMP

according to a procedure similar to that of plasma TEOS oxide film 4.

An upper interconnection not shown connected to metal interconnection 3 via a contact hole (via hole) is formed on plasma TEOS oxide film 9. Since the planarization of interlayer insulation film 10 formed of plasma TEOS oxide film 4, organic SOG film 5, modified SOG film 7, plasma TEOS oxide film 8 and plasma TEOS oxide film 9 can be set extremely favorable, the process of forming the upper interconnection can be carried out more easily. Also, the probability of disconnection in the upper interconnection can be reduced significantly.

Fourth Embodiment

A fabrication method of a semiconductor device according to a fourth embodiment of the present invention will be described hereinafter with reference to Figs. 15-19. The fabrication method of the fourth embodiment differs from the fabrication method of the first embodiment only in the step corresponding to the fourth to seventh steps of the first embodiment shown in Figs. 4-7. The prior steps corresponding to the first to third steps are identical. Therefore, only the different steps will be described, and description of the other similar steps will not be repeated.

A structure as shown in Fig. 3 is completed according

to a process similar to that of the first embodiment shown in Figs. 1-3. Then, a photoresist film 11 is applied on organic SOG film 5 as shown in Fig. 15. Photoresist film 11 is formed so as to alleviate the step-graded portion on the substrate similar to organic SOG film 5. More specifically, photoresist film 11 is formed thick at a concave portion and thin at a convex portion. Therefore, the surface thereof is extremely flat.

Then, argon ions (Ar^+) 6 are introduced by ion implantation to organic SOG film 5 as shown in Fig. 16. This ion implantation is carried out under the condition that only the surface layer (the portion above the topmost plane of plasma TEOS oxide film 4) through photoresist film 11. The portion implanted with ions is modified into SOG film 7.

The depth of the ions implanted is substantially uniform when ion implantation is carried out through photoresist film 11 since the surface thereof is extremely flat. Therefore, the bottom face of the modified region of the organic SOG film is planarized. Photo resist film 11 is preferably formed of a material having an implantation range substantially equal to that of organic SOG film 5.

Following the above ion implantation, photoresist film 11 is removed by ashing. Then, a plasma TEOS oxide film 8 is formed on modified SOG film 7 (organic SOG film

5) as shown in Fig. 17.

By polishing the surface of the device formed by the above steps until plasma TEOS oxide film 4 is exposed by CMP, a structure as shown in Fig. 18 is obtained. Since the lower face of modified SOG 7 is extremely flat, organic SOG film 5 not modified is exposed due to its low polishing rate simultaneous to the exposure of plasma TEOS oxide film 4. This organic SOG film 5 serves as a polish stopper to facilitate detection of the end point of polishing.

Then, a plasma TEOS oxide film 9 is formed on the surface of the polish device as shown in Fig. 19. An upper interconnection not shown connected to metal interconnection 3 via a contact hole (via hole) is formed on plasma TEOS oxide film 9.

Although adjustment is provided so that modified SOG film 7 and plasma TEOS oxide film 8 have substantially an equal polishing rate in the above embodiments, the expected object of the present invention is to facilitate polishing of organic SOG film 5. The inventors of the present invention confirmed the relationship between the wettability of organic SOG film 5 and the polishing rate by CMP according to experiments. The contact angle θ of purified water (having a resistivity of 18 MΩ•cm at 25°C) on an organic SOG film was measured so as to indicate the

wettability of the organic SOG film. This contact angle is the angle θ between a drop of purified water on the organic SOG film and the underlying film (SOG film).

Fig. 25 shows the polishing rate of five organic SOG films having different contact angles (solid circle in drawing), and the relationship between the contact angle and the polishing rate of each film when ions are implanted into each organic SOG film under the same condition (open circle in drawing).

It is appreciated that the polishing rate is increased as the contact angle becomes smaller from the border of 30°C. This phenomenon is probably due to the fact that the great amount of the methyl group in the organic SOG film responsible for low wettability is decomposed by ion implantation to result in better wettability. More specifically, a high polishing rate can be obtained by implanting ions into the organic SOG film to set the contact angle to be not more than 30°C.

The wettability (contact angle) of the organic SOG film (modified SOG film) can be adjusted by altering the dosage. For example, by setting the contact angle to 25°C, a polishing rate of a level identical to that of the plasma TEOS oxide film (PE-TEOS) and the thermal oxide film (th-SiO_2) can be obtained.

Fifth Embodiment

In the first to fourth embodiments, the polishing rate of organic SOG film 5 (modified SOG film 7) can be increased by implanting ions to organic SOG film 5. In the fifth embodiment of the present invention, the polishing rate of organic film 5 can be increased by improving the wettability of the employed abrasive liquid per se on organic SOG film 5. Abrasive liquid having a small contact angle when dropped on organic SOG film 5 is used to improve the wettability of the abrasive liquid per se with respect to organic SOG film 5.

Abrasive liquid of favorable wettability can be obtained by adding 0.1-0.5mol/ℓ, for example, of a surfactant (for example, a fatty acid compound such as formic acid, acetic acid, propionic acid, and butyric acid) into the abrasive liquid (an abrasive such as silica suspended in potassium hydroxide aqueous solution or ammonia aqueous solution) used in the previous first to fourth embodiments.

Modified SOG film 7 has the advantage that the film becomes less hygroscopic as well as moisture being removed therefrom, in addition to the increase in the polishing rate. Therefore, ions should be implanted into organic SOG film 5 after CMP in order to enjoy the above advantages.

Sixth Embodiment

A fabrication method of a semiconductor device according to a sixth embodiment of the present invention will be described hereinafter with reference to Figs. 26-32. The sixth embodiment differs from the previous first to fifth embodiments in that impurity ions are implanted after the polish operation by CMP. Components identical to those of the first embodiment have the same reference characters allotted, and detailed description thereof will not be repeated.

Referring to Fig. 26, a silicon oxide film 2 is formed on the surface of silicon substrate 1. A metal interconnection 3 is formed on silicon oxide film 2.

Referring to Fig. 27, a plasma TEOS oxide film 4 is formed on metal interconnection 3.

Referring to Fig. 28, an organic SOG film 5 is formed on plasma TEOS oxide film 4.

Referring to Fig. 29, a plasma TEOS oxide film 8 is formed to a thickness of 1-2μm on organic SOG film 5 according to a procedure similar to that of plasma TEOS oxide film 4.

Referring to Fig. 30, the surface of the device formed according to the above steps is polished by CMP. Here, a slurry including a surfactant is used as the abrasive liquid. This polish operation by CMP is terminated before plasma TEOS oxide film 4 is exposed as

shown in Fig. 30.

Referring to Fig. 31, argon ions (Ar^+) are doped to the surface of organic SOG film 5 by ion implantation. This ion implantation is carried out under the conditions so that ions are implanted at least to the portion exposed at the time of formation of a via hole. Modifying organic SOG film 5 by implanting ions to the portion that will be exposed at the time of via hole formation provides the advantage of preventing contact failure in forming an electrode in a via hole caused by gas from the SOG film when exposed at the sidewall of the via hole formed at a subsequent step.

Referring to Fig. 32, a plasma TEOS oxide film 9 is formed to a thickness of approximately 200nm, for example, on the film planarized by CMP by a procedure similar to that of plasma TEOS oxide film 4 for the purpose of preventing any adverse effect from the moisture in the atmosphere and to further increase the mechanical strength as an interlayer insulation film.

An upper interconnection not shown connected to metal interconnection 3 via a contact hole (via hole) is formed on plasma TEOS oxide film 9.

Since the planarization of interlayer insulation film 10 formed of plasma TEOS oxide film 4, organic SOG film 5, modified SOG film 7, plasma TEOS oxide film 8 and plasma

TEOS oxide film 9 can be made favorable, the process for forming the upper layer interconnection can be carried out more easily. Also, the probability of disconnection in the upper layer interconnection can be reduced.

The present invention is not limited to the above-described embodiment. Similar advantages can be achieved by implementation as set forth in the following.

(1) Polyimide or polyimide composed with siloxane can be used instead of organic SOG film 5.

(2) An inorganic SOG film can be used instead of organic SOG film 5 to which ion implantation is carried out thereto. This provides the advantage that the moisture and hydroxyl group included in the inorganic SOG film can be reduced.

(3) A silicon oxide film formed by a method other than plasma CVD (such as atmospheric CVD, low pressure CVD, ECR plasma CVD, photoexcitation CVD, TEOS-CVD, PVD) can be used instead of the silicon oxide films of plasma TEOS oxide film 4, 8 and 9. In this case, the gas used in the atmospheric pressure CVD method is monosilane and oxygen (SiH_4+O_2). The film growth temperature is not more than 400°C. The gas used for low pressure CVD is monosilane and nitrous oxide (SiH_4+N_2O). The film growth temperature thereof is not more than 900°C.

(4) Each of plasma TEOS oxide films 4, 8 and 9 can be

replaced with another insulation film (such as silicon nitride film and silicate glass film) having a high mechanical strength in addition to the property for blocking moisture and the hydrogen group. This insulation film can be formed by an arbitrary method such as CVD and PVD.

(5) In the above-described embodiments, argon ions are used for ion implantation into organic SOG film 5. However, any ion that can modify the property of organic SOG film 5 can be used. More specifically, ion of a relatively small mass such as argon, boron, nitrogen and phosphorus is suitable. Additionally, the following ions can be expected to provide sufficient effects.

① Inert gas ions other than argon (such as helium ion, neon ion, krypton ion, xenon ion and radon ion) can be used. Since inert gas does not react with the organic SOG film, there is no probability of advert influence by ion implantation.

② Element unitary ions of the groups IIIb, IVb, Vb, VIb and VIIb other than boron and nitrogen, and compound ions thereof can be used. Particularly, the element unitary ions and compound ions of oxygen, aluminum, sulfur, chlorine, gallium, germanium, arsenic, selenium, bromine, antimony, iodine, indium, tin, tellurium, lead, and bismuth preferably can be used.

Particularly, metal element ions can suppress the dielectric constant to a low level for organic SOG film 5 subjected to ion implantation.

③ Element unitary ions of the groups IVa, Va, and compound ions thereof can be used. Particularly, element unitary ions of titanium, vanadium, niobium, hafnium, and tantalum and compound ions thereof are preferable. Since the dielectric constant of the oxide of the element of the groups IVa and Va is high, the dielectric constant of organic SOG film 5 subjected to ion implantation increases. However, this is of no particular problem in practice except for the cases where an interlayer insulation film of a low dielectric constant is required.

④ A plurality of types of the above-described ions can be used in combination. In this case, a further superior effect can be obtained by the synergism of each ion.

(6) Modified SOG film 7 can be subjected to a heat treatment. In this case, the number of dangling bonds in modified SOG film 7 is reduced to result in a lower hygroscopic property. Therefore, moisture permeability is further reduced.

(7) In the above-described embodiments, ions are implanted into organic SOG film 5. The present invention is not limited to ions, and electrons, atoms, molecules,

or particles can be introduced. In the present invention, these are generically referred to as "impurities".

(8) Modified SOG film 7 is extremely superior than organic SOG film 5 in hygroscopic property, water resistance, and mechanical strength. Therefore, plasma TEOS oxide film 9 can be omitted appropriately in each of the above-described embodiments.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A fabrication method of a semiconductor device comprising the steps of:

introducing impurities into a first insulation film, and

effecting planarization by polishing a surface of said first insulation film after said impurities are introduced.

2. A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation film on a substrate,

forming a second insulation film on said first insulation film,

introducing impurities at least to a surface of said first insulation film either before or after forming said second insulation film, and

effecting planarization by polishing at least said second insulation film.

3. The fabrication method of a semiconductor device according to claim 2, wherein said step of planarization comprises the step of effecting planarization by polishing said first and second insulation films.

4. The fabrication method of a semiconductor device according to claim 2, wherein said second insulation film includes a silicon oxide film formed by plasma CVD.

5. The fabrication method of a semiconductor device according to claim 2, wherein said step of introducing impurities comprises the steps of

forming a photoresist on a surface of a device before impurities are introduced to said first insulation film, and

introducing impurities into said first insulation film via said photoresist film.

6. The fabrication method of a semiconductor device according to claim 2, further comprising the step of forming a third insulation film on a surface of a device after said polishing.

7. The fabrication method of a semiconductor device according to claim 2, further comprising the step of forming a fourth insulation film on a surface of a device before said first insulation film is formed.

8. The fabrication method of a semiconductor device

according to claim 2, wherein said first insulation film includes a silicon oxide material containing at least 1% of carbon.

9. The fabrication method of a semiconductor device according to claim 2, wherein said first insulation film includes a material having a contact angle of not more than 30° of purified water with respect to said first insulation film.

10. The fabrication method of a semiconductor device according to claim 2, wherein said first insulation film includes an inorganic SOG film.

11. The fabrication method of a semiconductor device according to claim 2, wherein said polishing is carried out by chemical mechanical polishing.

12. The fabrication method of a semiconductor device according to claim 11, wherein a surfactant is used in said polishing step.

13. The fabrication method of a semiconductor device according to claim 2, wherein said step of introducing impurities comprises the step of introducing impurities

into said first insulation film by implantation.

14. The fabrication method of a semiconductor device according to claim 13, wherein said impurities include at least one element selected from the group consisting of argon, boron, nitrogen and phosphorus.

15. A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation film on a substrate,

introducing impurities at least to a surface of said first insulation film, and

effecting planarization by polishing said first insulation film.

16. The fabrication method of a semiconductor device according to claim 15, wherein said step of introducing impurities comprises the step of introducing impurities only to a surface of said first insulation film.

17. The fabrication method of a semiconductor device according to claim 15, further comprising the step of forming a third insulation film on a surface of a device after said polishing.

18. The fabrication method of a semiconductor device according to claim 15, further comprising the step of forming a fourth insulation film on a surface of a device before said first insulation film is formed.

19. The fabrication method of a semiconductor device according to claim 15, wherein said first insulation film includes a silicon oxide material containing at least 1% of carbon.

20. The fabrication method of a semiconductor device according to claim 15, wherein said first insulation film includes a material having a contact angle of not more than 30° of purified water with respect to said first insulation film.

21. The fabrication method of a semiconductor device according to claim 15, wherein said first insulation film includes an inorganic SOG film.

22. The fabrication method of a semiconductor device according to claim 15, wherein said polishing is carried out according to chemical mechanical polishing.

23. The fabrication method of a semiconductor device

according to claim 15, wherein a surfactant is used in said polishing step.

24. The fabrication method of a semiconductor device according to claim 15, wherein said step of introducing impurities comprises the step of introducing impurities into said first insulation film by implantation.

25. The fabrication method of a semiconductor device according to claim 15, wherein said impurities include at least one element selected from the group consisting of argon, boron, nitrogen and phosphorus.

26. The fabrication method of a semiconductor device comprising the steps of:

forming a first insulation film on a substrate,

forming a second insulation film on said first insulation film, and

effecting planarization by polishing at least said second insulation film by chemical mechanical polishing using an abrasive liquid including a surfactant.

27. The fabrication method of a semiconductor device according to claim 26, wherein said surfactant includes a fatty acid compound.

28. The fabrication method of a semiconductor device according to claim 26, further comprising the step of introducing impurities into said first insulation film after said polishing step.

29. An abrasive liquid including at least a surfactant used for a chemical mechanical polishing process.

30. The abrasive liquid according to claim 29, wherein said surfactant includes a fatty acid compound.

ABSTRACT OF THE DISCLOSURE

A fabrication method of a semiconductor device improved in the polishing rate of an insulation film and less likely to generate a defect during polishing is obtained. In this fabrication of a semiconductor device, impurities are introduced into a first insulation film, and then planarization is effected by polishing the surface of the first insulation film. Thus, the polishing rate of the portion of the first insulation film in which impurities are introduced is improved. Also a defect is not easily generated therein.

A, W, H, McL & N Docket No._____ ARMSTRONG, WESTERMAN, HATTORI, MCLELAND & NAUGHTON

Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention **entitled**
(Insert Title) Fabrication Method of Semiconductor Device and Abrasive Liquid Used Therein
the specification of which is attached hereto unless the following is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a) - (d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

	(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
(List prior foreign applications. See note A on back of this page)	8-230826(P)	Japan	30/August/1996	☒ Yes ☐ No
	9-010426(P)	Japan	23/January/1997	☒ Yes ☐ No
				☐ Yes ☐ No
				☐ Yes ☐ No

(See note B on back of this page) ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of the application:

	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)
(List Prior U.S. Applications)			

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

James E. Armstrong, III, Reg. No. 18,366; William F. Westerman, Reg. No. 29,988; Ken-Ichi Hattori, Reg. No. 32,861; Le-Nhung McLeland, Reg. No. 31,541; Ronald F. Naughton, Reg. No. 24,616; John R. Pegan, Reg. No. 18,069; William G. Kratz, Jr., Reg. No. 22,631; Albert Tockman, Reg. No. 19,722; Mel R. Quintos, Reg. No. 31,898; Donald W. Hanson, Reg. No. 27,133; Stephen G. Adrian, Reg. No. 32,878; William L. Brooks, Reg. No. 34,129; John F. Carney, Reg. No. 20,276; Edward F. Welsh, Reg. No. 22,455; Patrick D. Muir, Reg. No. 37,403; Gay A. Spahn, Reg. No. 34,978; and John P. Kong, Reg. No. 40,054.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

(See note C above)

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Inventor's Signature Yasunori Inoue Date July 17, 1997

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Inventor's Signature Yoshio Okayama Date July 17, 1997

Residence Gifu, Japan Citizenship Japanese

Post Office Address 2-54, Oi-cho, Ogaki-shi, Gifu, Japan

Full name of third inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of fourth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of fifth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of sixth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of seventh inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of eighth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Fig.1

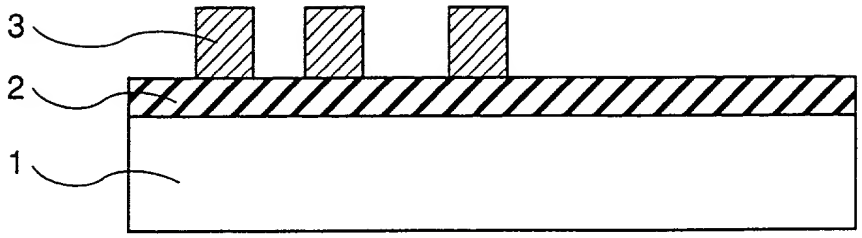

Fig.2

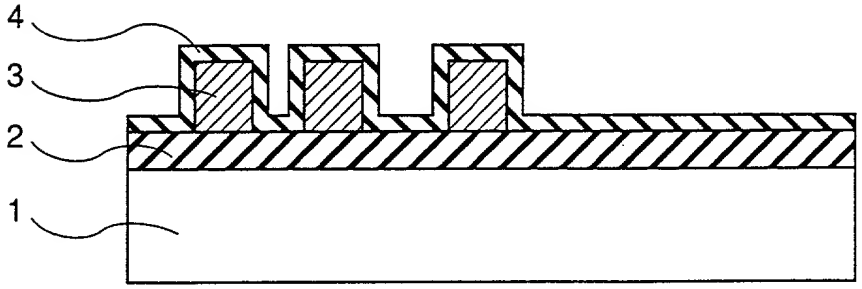

Fig.3

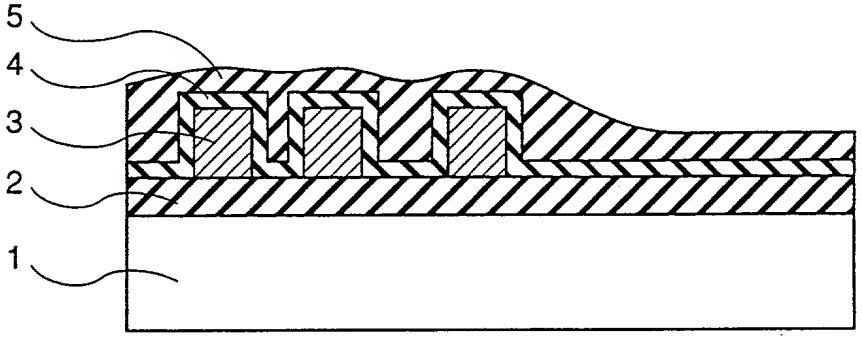

Fig.4

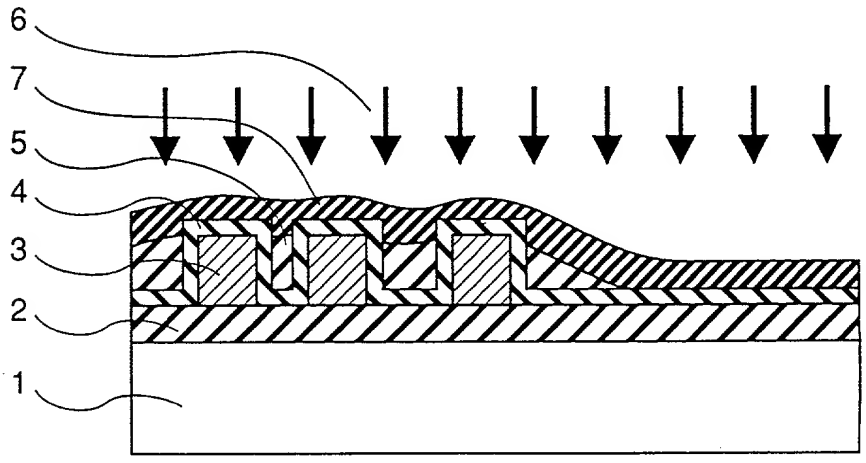

Fig.5

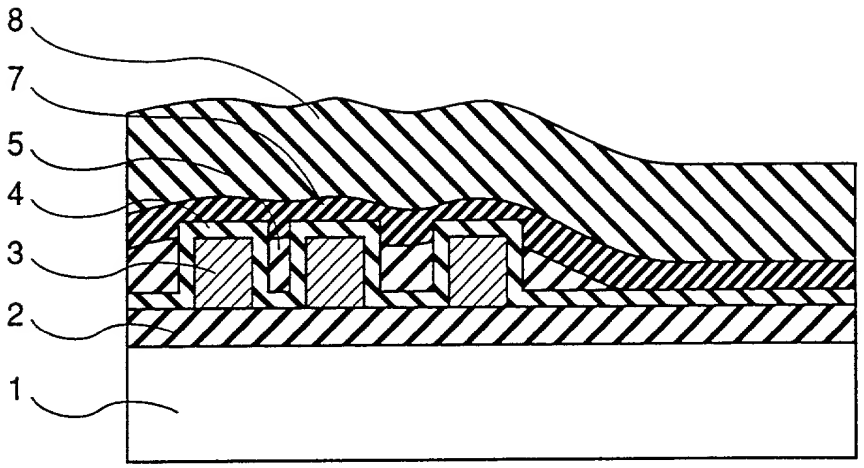

Fig.6

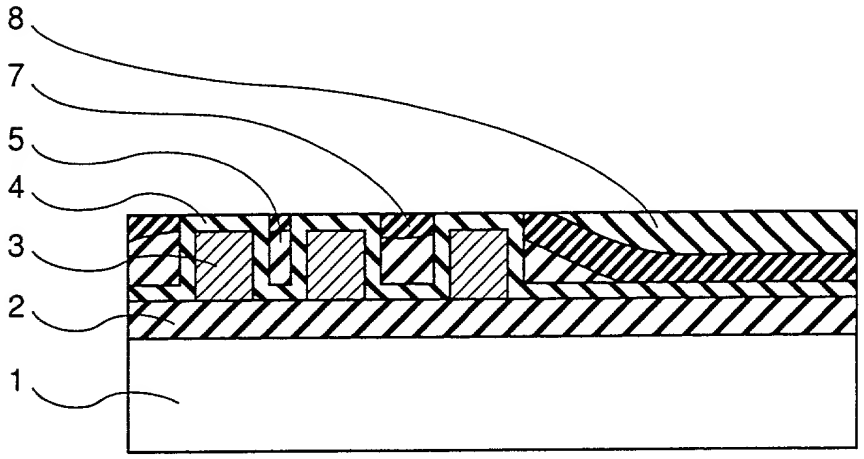

Fig.7

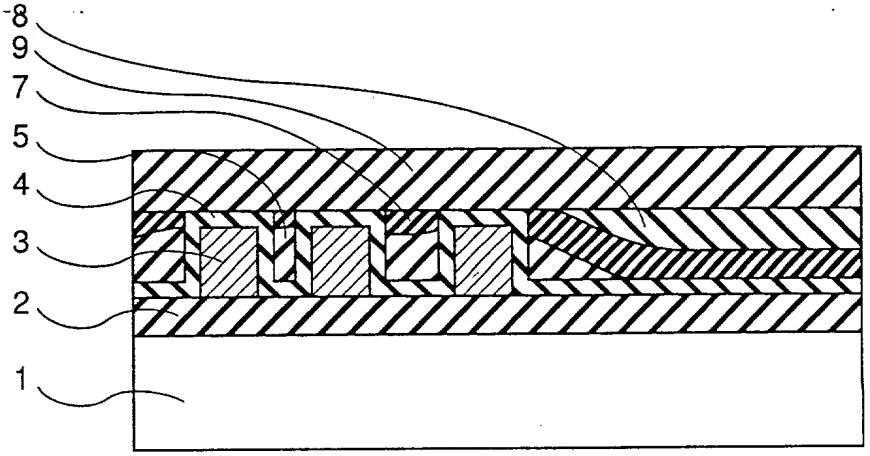

Fig.8

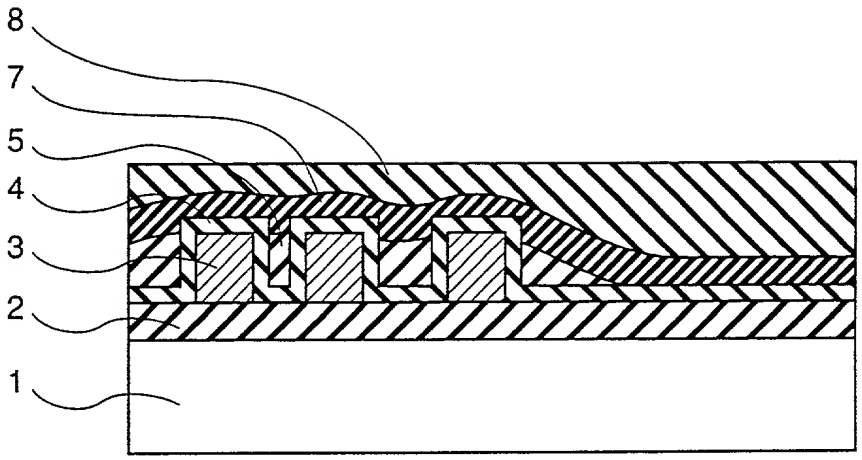

Fig.9

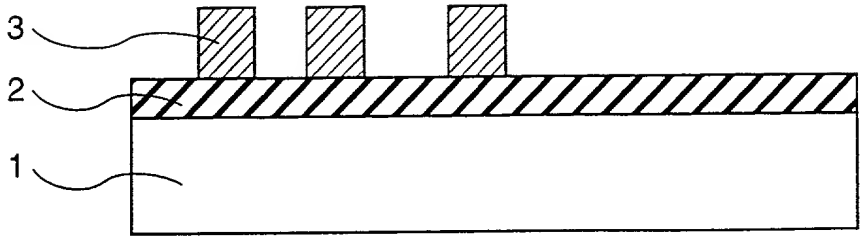

Fig.10

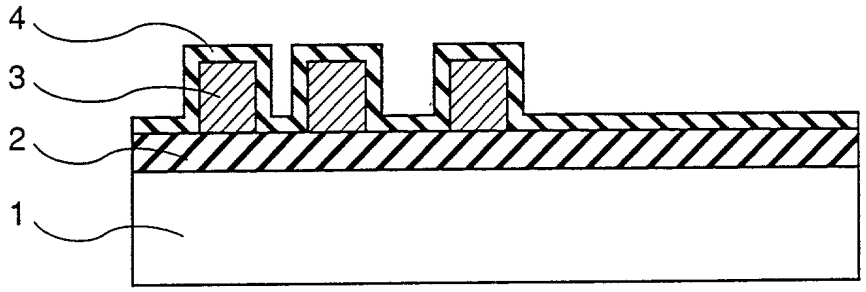

Fig.11

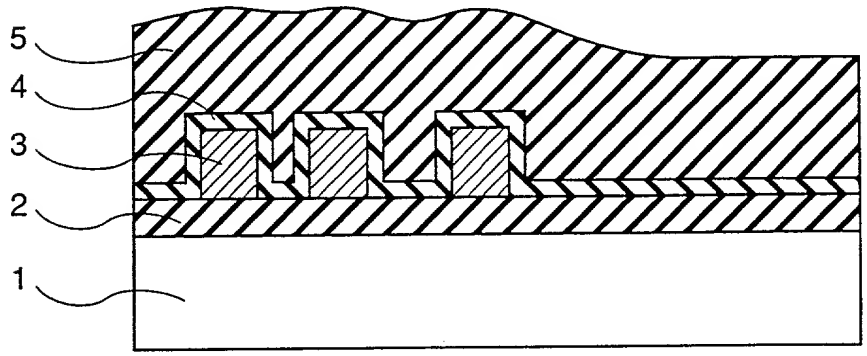

Fig.12

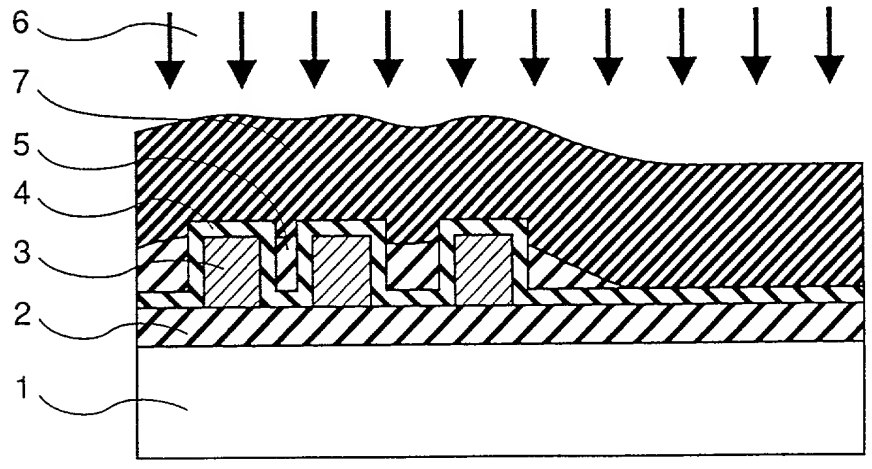

Fig.13

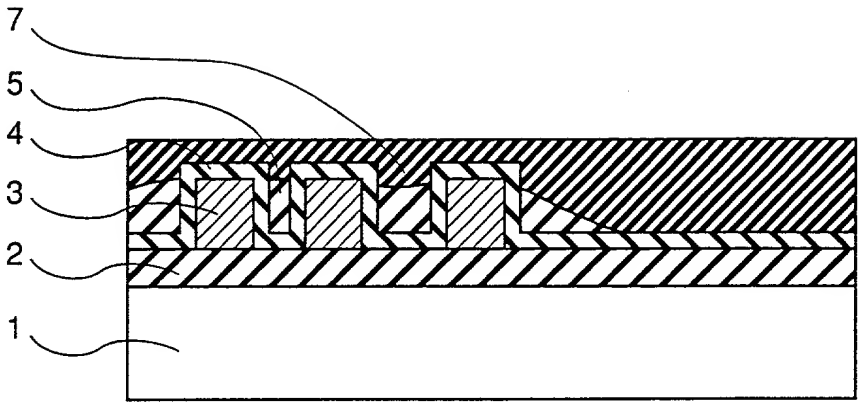

Fig.14

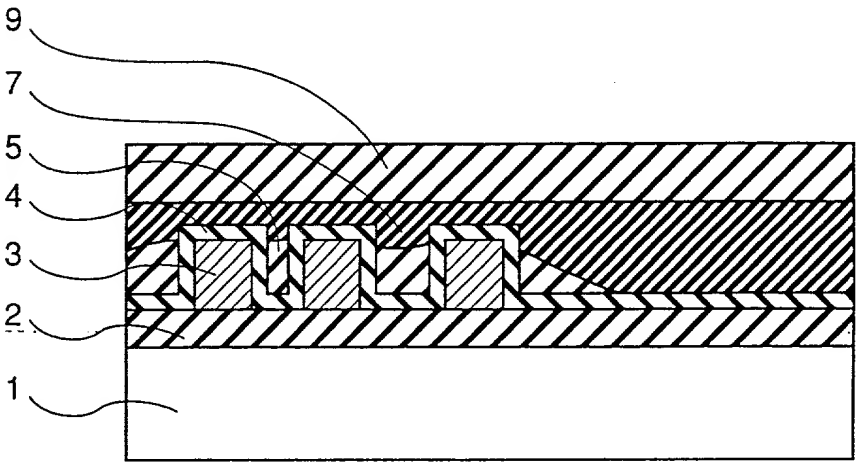

Fig.15

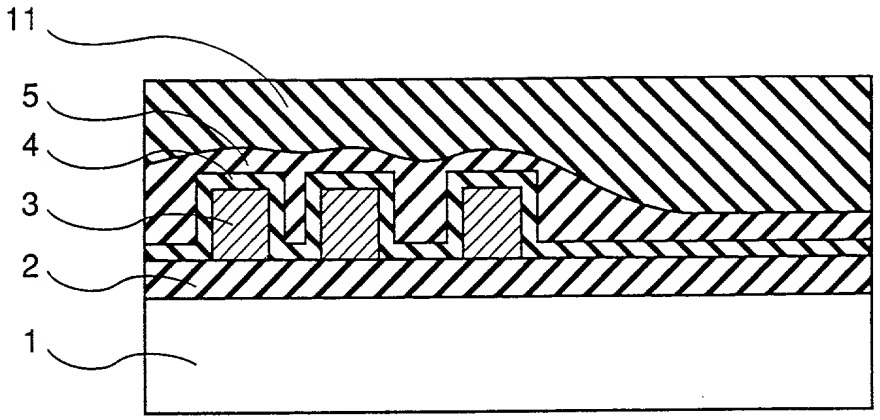

Fig.16

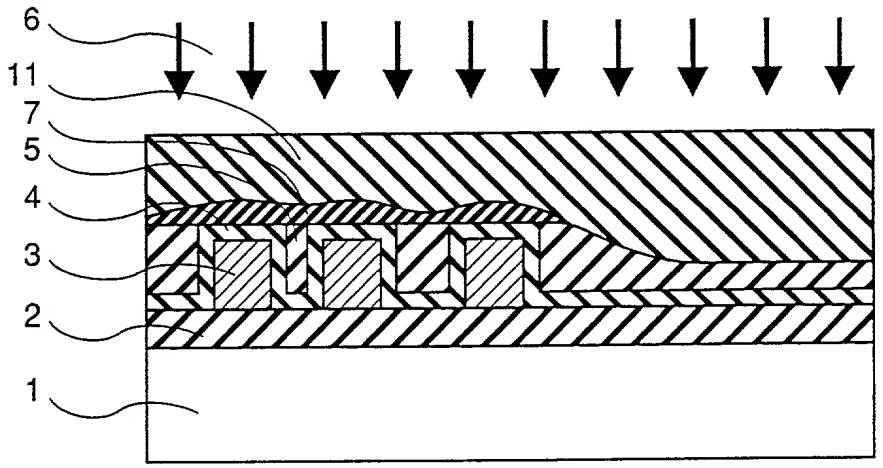

Fig.17

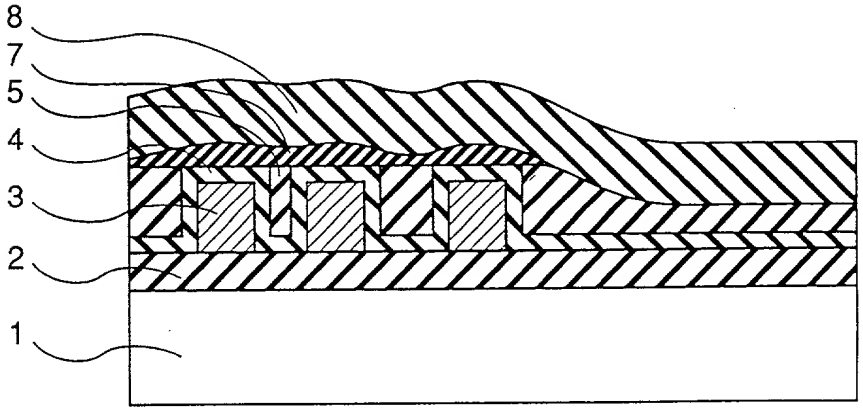

Fig.18

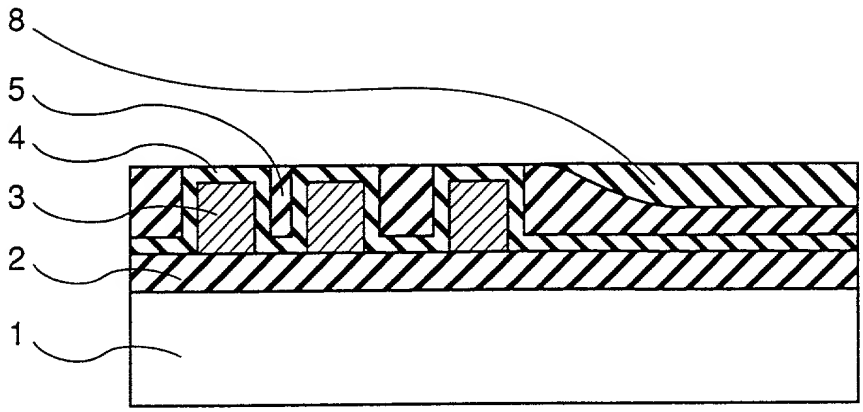

Fig.19

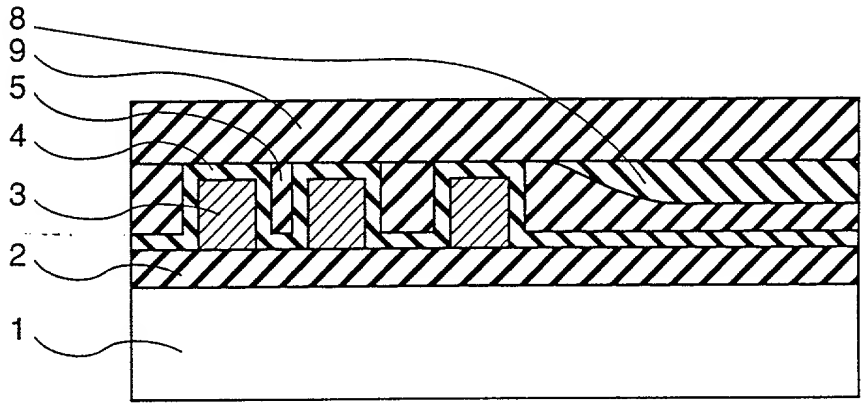

Fig.20

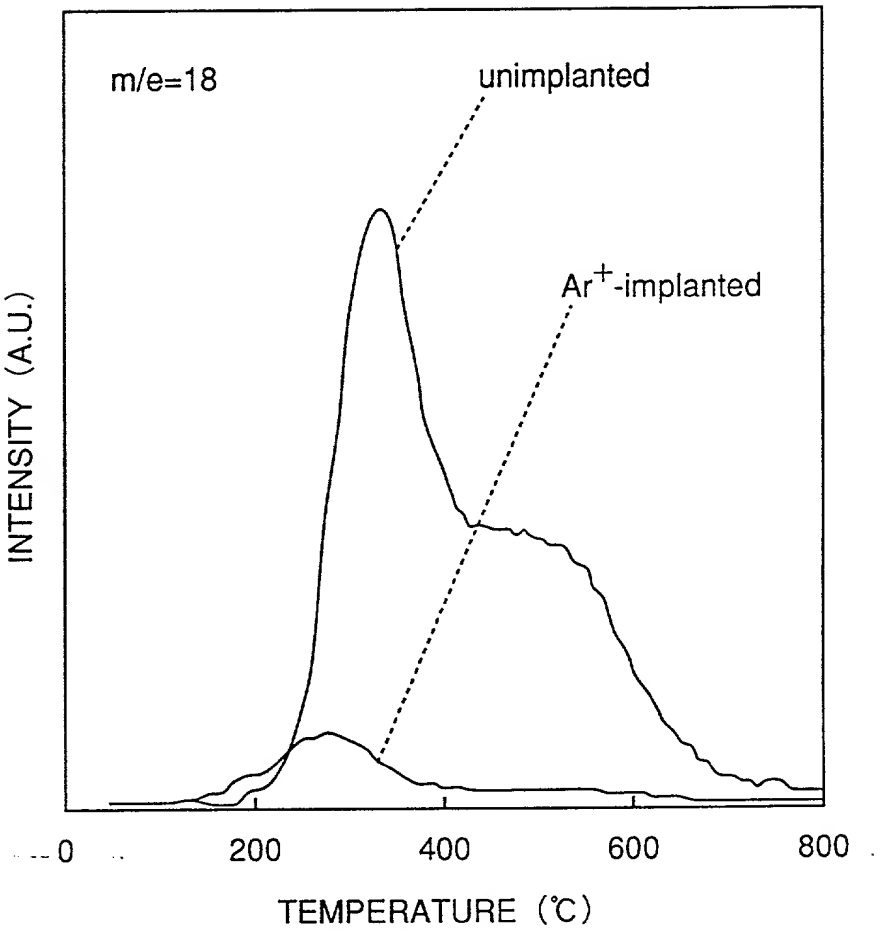
m/e=18
unimplanted
Ar+-implanted
INTENSITY (A.U.)
0
200
400
600
800
TEMPERATURE (℃)

Fig.21

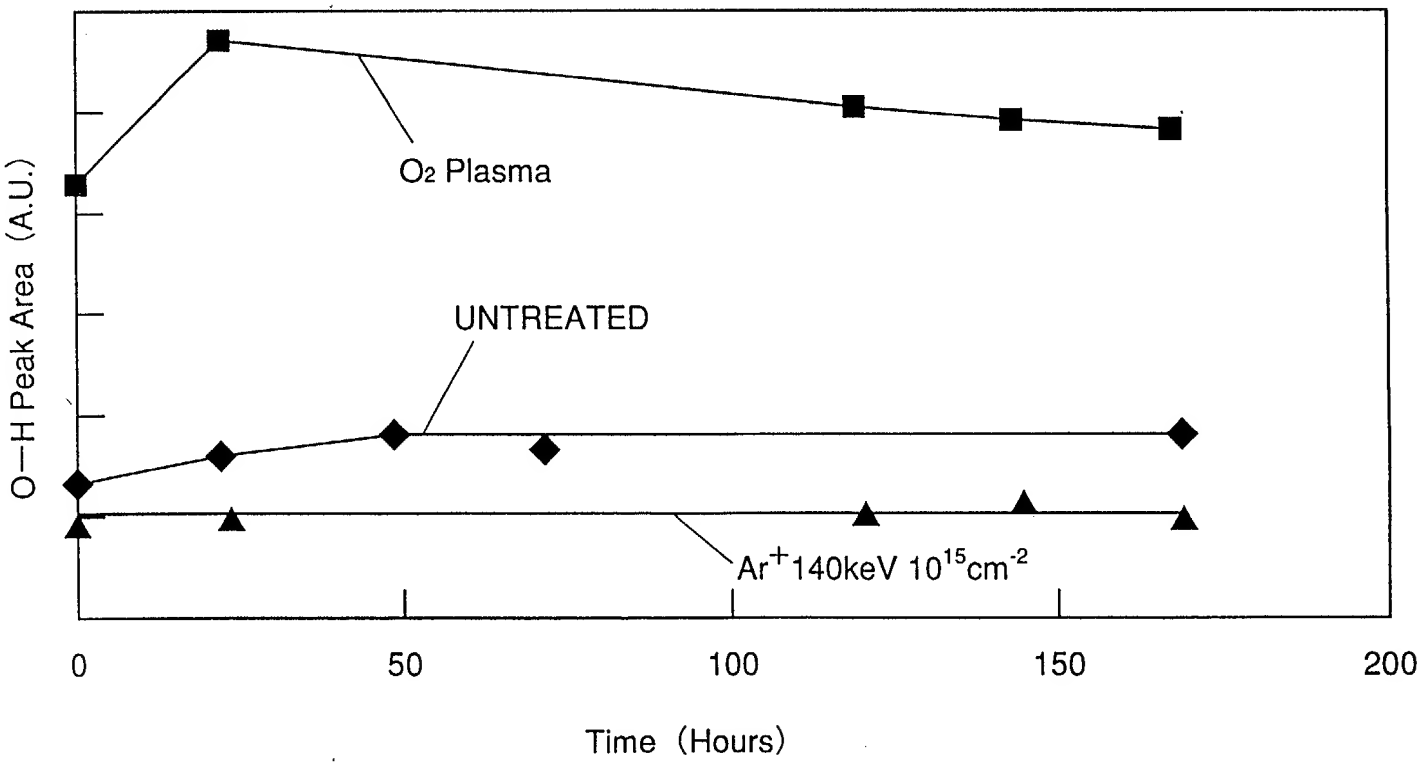
O—H Peak Area (A.U.)
O2 Plasma
UNTREATED
Ar+140keV 10^15cm^-2
0
50
100
150
200
Time (Hours)

Fig.22

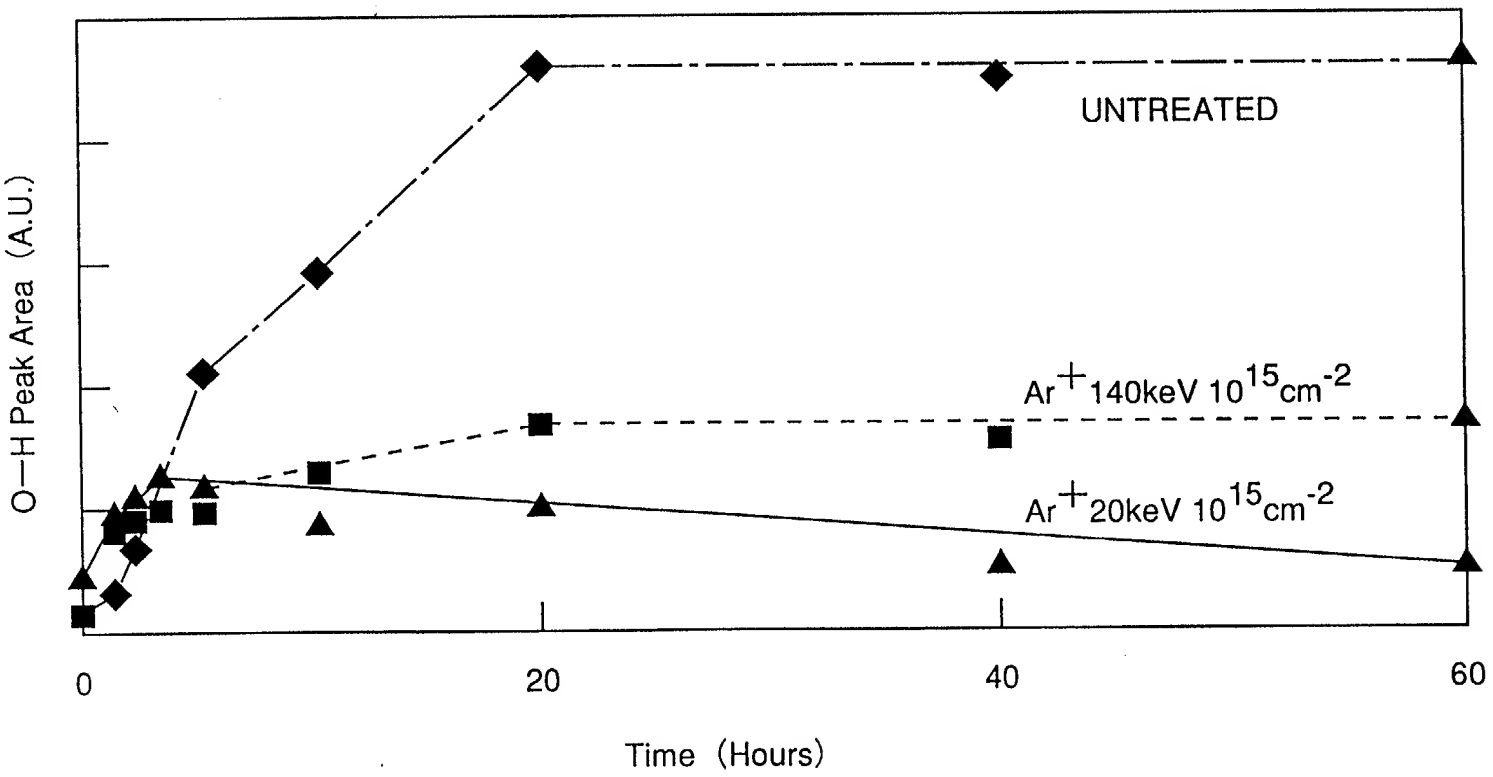
UNTREATED
Ar+140keV 10^15cm^-2
Ar+20keV 10^15cm^-2
O—H Peak Area (A.U.)
0
20
40
60
Time (Hours)

Fig.23

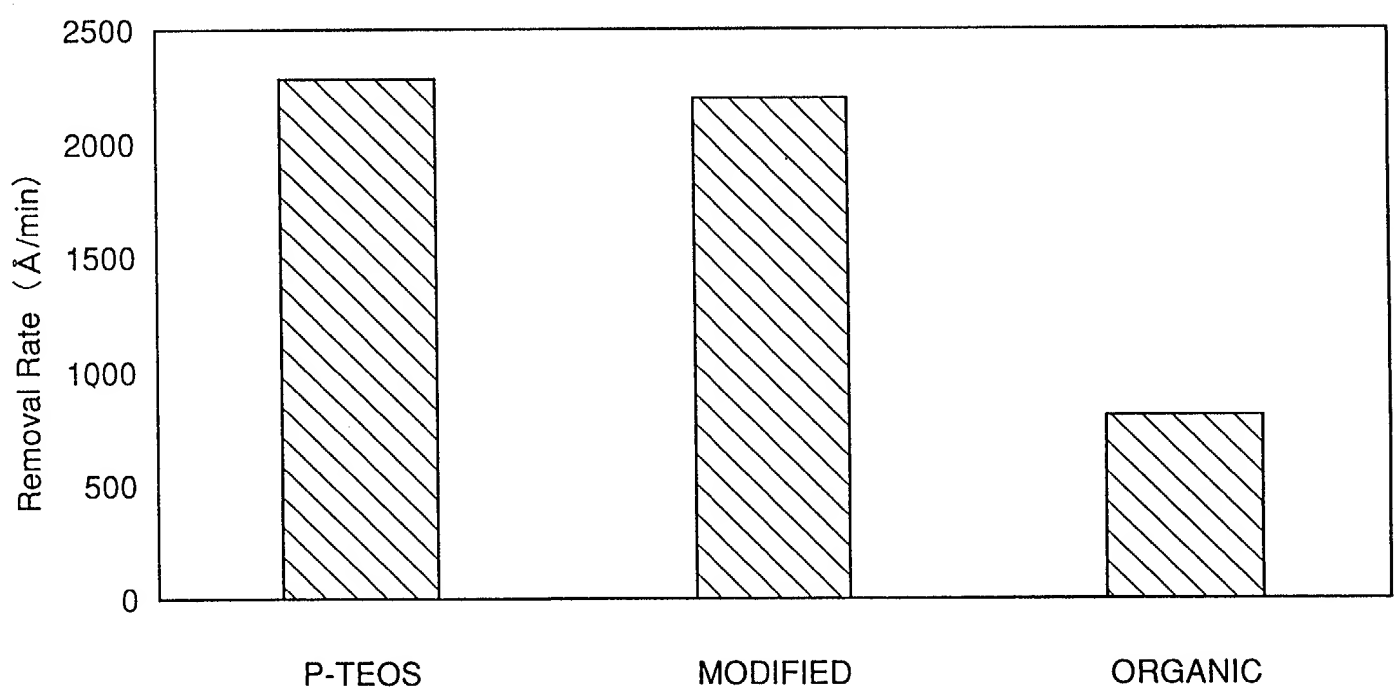
2500
2000
1500
1000
500
0
Removal Rate（Å/min）
P-TEOS
MODIFIED
ORGANIC

Fig.24

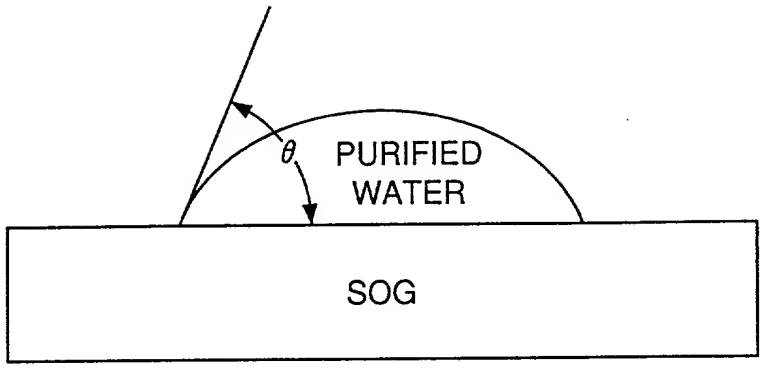
θ
PURIFIED
WATER
SOG

Fig.25

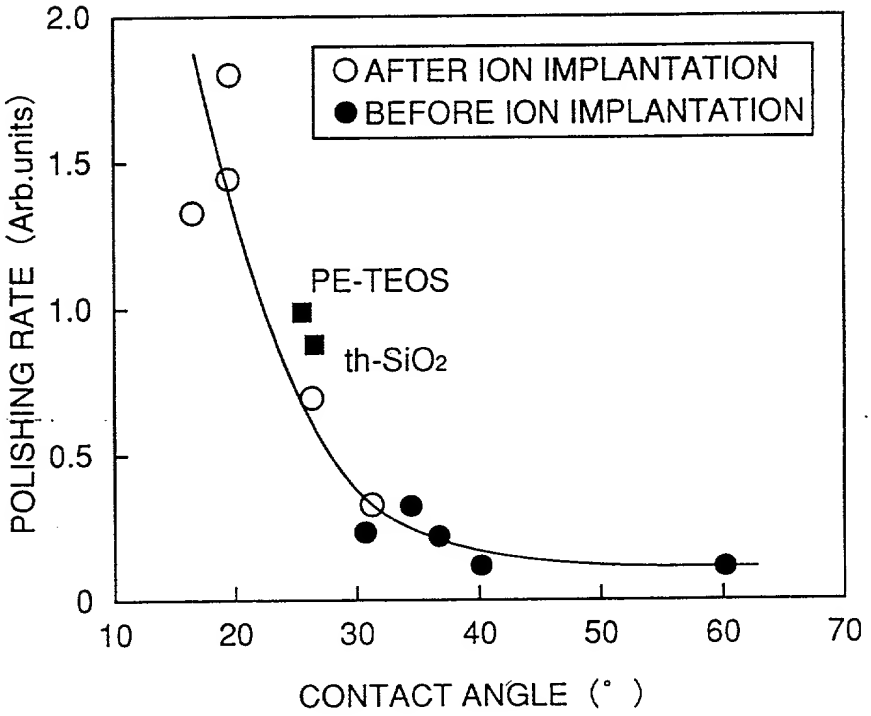
2.0
1.5
1.0
0.5
0
POLISHING RATE (Arb.units)
○AFTER ION IMPLANTATION
●BEFORE ION IMPLANTATION
PE-TEOS
th-SiO2
10
20
30
40
50
60
70
CONTACT ANGLE (°)

Fig.26

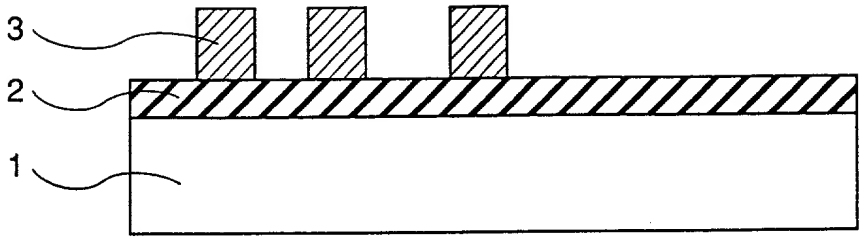

Fig.27

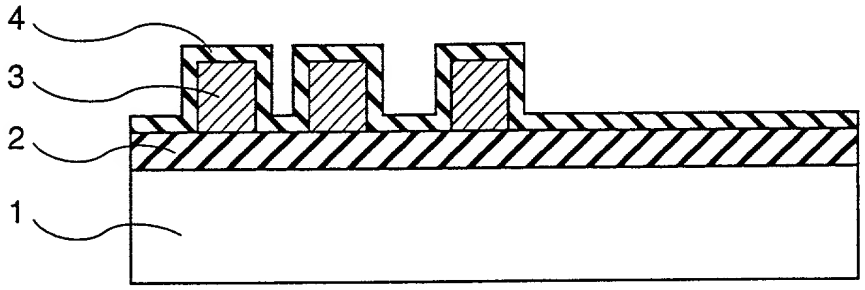

Fig.28

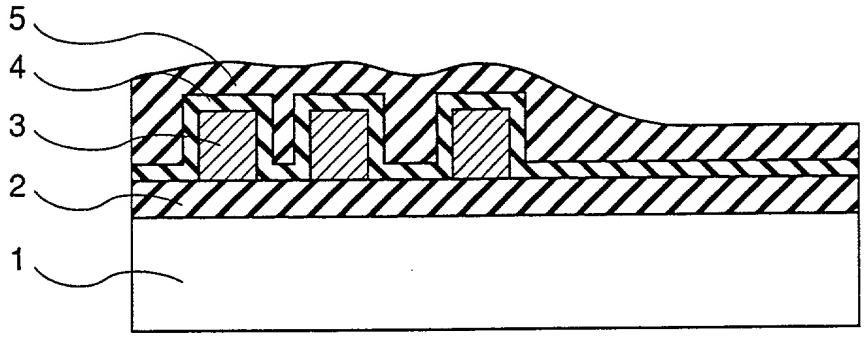

Fig.29

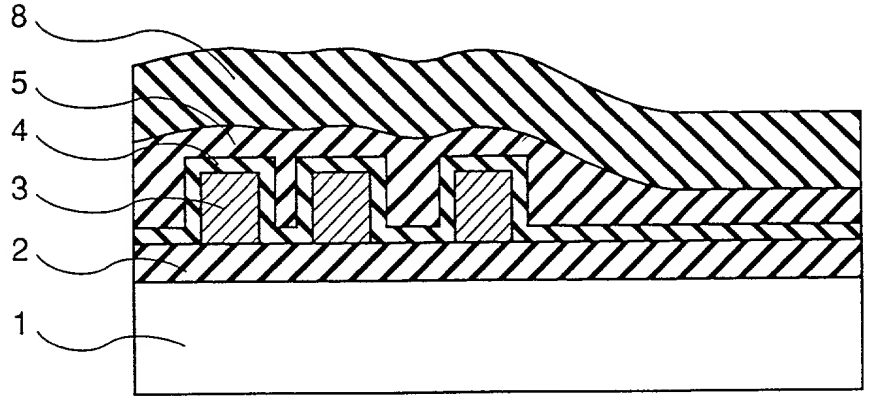

Fig.30

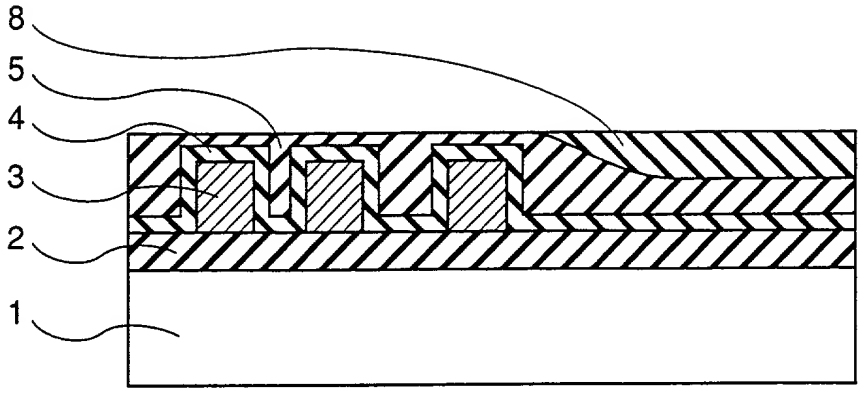

Fig.31

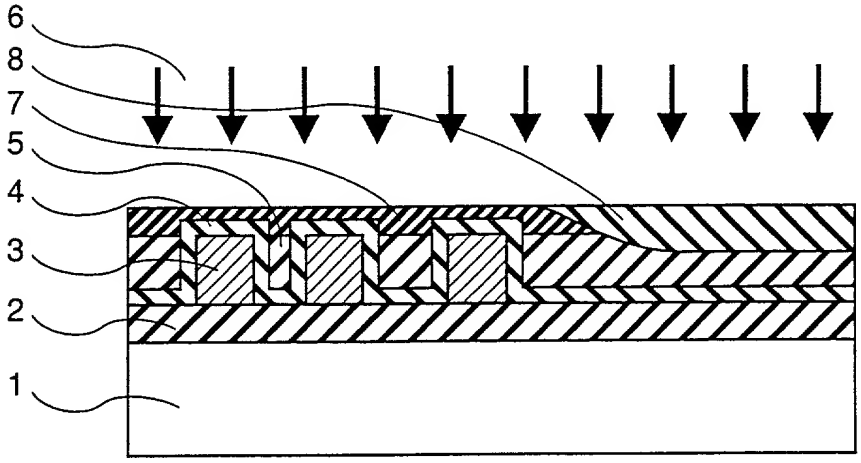

Fig.32